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(54) Method for manufacturing a semiconductor structure comprising regions formed with low dielectric constant material

(57) An interconnect structure having a dielectric layer with low dielectric constant is formed within an integrated circuit. In one embodiment of the invention, portions of a silicon dioxide layer (18) lying adjacent to a conductive interconnect (21) are removed to expose portions of a silicon nitride etch stop layer (16). A dielectric layer (22) having a low dielectric constant is then formed overlying the conductive interconnect (21) and the exposed portions of the silicon nitride etch stop layer (16). A portion of the dielectric layer (22) is then removed to expose the top surface of the conductive interconnect (21) to leave portions of the dielectric layer (22) between adjacent conductive interconnects (21). The resulting interconnect structure has reduced cross-talk between conductive interconnects (21) while avoiding prior art disadvantages of reduced thermal dissipation and increased mechanical stress.

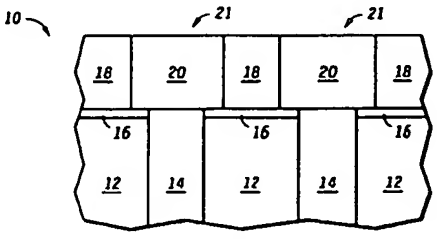

FIG.3

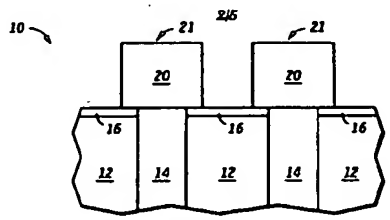

FIG.4

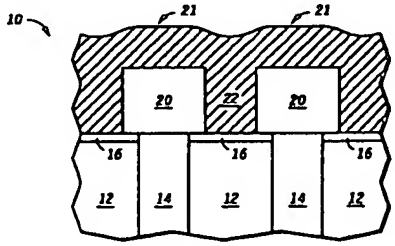

FIG.5

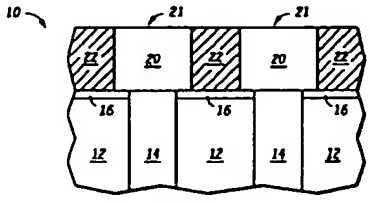

FIG.6

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ously sealed by the second dielectric layer. A dual in-laid metal interconnect is then formed within the contact opening whereby the low-K second dielectric is positioned between conductive regions where isolation benefits are achieved while thermal and mechanical properties are improved.

In an alternative embodiment of the invention, void/air regions are formed between adjacent conductive metal interconnect lines by spinning on a polymeric resin having a stiff polymer backbone. This stiff backbone material forms air regions between closely spaced metal conductive members within the same conductive interconnect layer. Depending upon the atomic gas content of the air gaps and atmospheric pressure of formation, the air gaps will approach a dielectric constant e=1 which is the optimal dielectric constant for reduction of cross-talk and adverse capacitive coupling in polysilicon and metal interconnects.

In yet another embodiment of the invention, a non-conformal dielectric layer is formed overlying adjacent conductive interconnect lines such that a void/air region is formed between closely-spaced conductive interconnect lines within the same conductive interconnect level. A second dielectric layer is then formed overlying the non-conformal dielectric layer and planarized to form a completed inter-level dielectric. The second dielectric layer and the non-conformal conductive layer are then patterned to form a contact or via opening which is then filled with conductive material to form a conductive interconnect. The void region between the two adjacent conductive interconnect lines reduces cross-talk/capacitance between the two conductive interconnect lines so that circuit speed is improved and logical cross-talk errors are avoided.

The embodiments of the present invention can be further understood with reference to FIGs. 1-16.

FIGs. 1-6 illustrate, in cross-sectional form, process steps for making an interconnect structure in accordance with a first embodiment of the invention. Shown in FIG. 1 is a portion 10 of an integrated circuit structure comprising a first dielectric layer 12, an etch stop layer 16, and a second dielectric layer 18. In FIG. 1, first dielectric layer 12, etch stop layer 16, and second dielectric layer 18 are patterned using conventional lithographic and etching techniques. In a preferred embodiment, first dielectric layer 12, etch stop layer 16, and second dielectric layer 18 are simultaneously patterned and etched using a plasma etch chemistry comprising a fluorinated etch species. For example, the layers 12, 16, and 18 may be patterned in a plasma environment which is generated using etch gases such as CHF_3, CF_4, C_2F_6 and/or the like. It is important to note that this etch process defines a contact opening 14 within first dielectric layer 12 which allows a metallic conductive layer to be subsequently deposited within the contact opening of FIG. 1 to form a conductive contact portion 14. This subsequently deposited conductive layer is used to make electrical contact/interconnection to an underlying conductive region such as another metal layer or a doped semiconductive region within polysilicon layer or the semiconductor substrate. The doped region may be a bipolar electrode, a well contact, a source/drain, a thin film transistor (TFT) node or a like doped polysilicon or substrate portion. Polysilicon may be replaced with amorphous silicon, epitaxially grown silicon, or refractory silicided silicon-containing layers.

In one embodiment, first dielectric layer 12 and second dielectric layer 18 are formed using the same material. For example, first dielectric layer 12 and second dielectric layer 18 may be a layer of borophosphosilicate glass (BPSG), layers of plasma tetraethylorthosilicate (TEOS), phosphosilicate glass (PSG) layers, silicon dioxide, nitride layers, fluorinated oxide layers, or like dielectric materials. In another form, the dielectric layer 18 may be made of a different material from layer 12. First dielectric layer 12, second dielectric layer 18 are formed using conventional plasma deposition processes, low pressure chemical vapor position (LPCVD) processes, or the like. In one embodiment, etch stop layer 16 is a layer of plasma enhanced silicon nitride when the layers 12 and 18 are oxide. Alternatively, etch stop layer 16, which can also function as an anti-reflective coating (ARC) used in lithographic processing, may be a layer of silicon rich silicon nitride, aluminum nitride, or any dielectric layer which can be used as an etch-back stopping layer or a chemical mechanical polishing (CMP) stop layer. Also, silicon oxide nitride (SiON) or silicon rich SiON may be used as an etch stop or anti-reflective coating (ARC) layer herein.

In FIG. 2, another photoresist and etch process is used to form interconnect trenches within layer 18. The openings through layer 12 in FIG. 1 are contact openings to underlying material whereas the opening formed through layer 18 in FIG. 2 is an interconnect trench. To form the interconnect trenches of an in-laid metal (damascene) process, the second dielectric layer 18 is etched selective to etch stop layer 16 using an etch chemistry environment. This etch process defines an interconnect region 20 within second dielectric layer 18. It is important to note that dual in-laid metal processing can be performed in other similar ways than that illustrated in FIGs. 1-2. FIGs. 1-2 are intended to be representative of any method for forming dual in-laid structures having contact areas and interconnect trenches.

In FIG. 3, a conductive layer of material is then deposited within contact portion 14 and interconnect portion 20. This conductive layer of material is subsequently planarized by CMP and/or etch processing to form conductive interconnects 21. In one embodiment, conductive interconnects 21 are formed by first depositing a thin barrier layer within contact portion 14 and interconnect portion 20 followed by a thicker conductive layer which more completely fills conductive portion 14 and interconnect portion 20. It should be appreciated that interconnect 21 may be formed using conventional

constant of e = 2.6 The polyimide may be formed from either a poly(amic) acid solution or a fully imidized polyimide in FIG. 8. In general, the spin-on material used in FIG. 8 to make the layer 40 can be any material which has a substantially stiff polymer backbone so that the air regions 38 are at least partially formed in FIG. 8.

To avoid blistering of the air gap 38 of FIG. 8, an anneal step of the layer 40 should be performed in a thermal ramp manner. The ramp should start at less than 100°C and arrive, after a selected temperature ramp time period, at roughly 100°C to 300°C for solvent-removal annealing of the layer 40. A slower ramp thermal process will be more likely to avoid any blistering of the air gap 38 than a fast exposure to high temperatures. Also, a sub-atmospheric spin-on process can be used to create air gaps 38 with reduced pressure or fewer trapped molecules/atoms. This sub-atmospheric process can reduce blistering effects by eliminating a high density of atoms within the gap 38.

In FIG. 9, conventional photolithographic patterning and etching techniques are then used to pattern and etch reflective layer 42 and dielectric layer 40 to define interconnect portion 41 within dielectric layers and to reexpose contact portion 38 which are the air gaps 38 in FIG. 8. It is important to note that additional etching is not required to form a contact opening to an underlying metal interconnect or doped silicon region since the air gaps 38 were isolated in FIG. 8. In one embodiment, dielectric layer 40 is patterned using a plasma comprising oxygen, and photoresist mask 44 used to define the opening within dielectric layer 40 is removed at the same time that dielectric layer 40 is etched. Therefore, in this embodiment the etch process used to pattern dielectric layer 40 also simultaneously removes some or all of the photoresist mask 44 used to define the opening within dielectric layer 40.

In FIG. 10, a barrier layer 49 and a conductive film material are then formed within contact opening 38 and interconnect region 41. A portion of the barrier layer 49 and the conductive film material are then selectively removed to form conductive interconnects 48 of FIG. 10. In one embodiment, conductive interconnects 48 are formed using conventional plasma etching techniques. Alternatively, connective interconnects 48 may be formed using conventional chemical mechanical polishing (CMP) techniques. An etch stop layer 46 or anti-reflective coating (ARC) layer 46 is then formed overlying dielectric 40 and conductive interconnects 48. It should be appreciated that the process steps illustrated in FIGs. 7-10 may then be repeated in order to form an additional set of conductive interconnects overlying conductive interconnects 48 and thus, integrated circuits having multiple layers of interconnects can be formed with the present invention. Since the high-K or high dielectric constant material 40 is: (1) located only between regions 48 where isolation advantages result; and (2) not located over the entire wafer to degrade mechanical stability and thermal dissipation, the final structure of FIG. 10 has advantages over the prior art.

FIGs. 11-15 illustrate cross-sectional process steps for making an interconnect structure in accordance with an alternative embodiment of the invention. Shown in FIG. 11 is a portion 50 of an integrated circuit structure comprising a first dielectric layer 52 and a plurality of conductive interconnects 54. First, dielectric layer 52 is formed using conventional plasma or chemical vapor deposition (CVD) techniques and may be a layer of BPSG, PSG, TEOS, fluorinated silicon oxide, or the like. The plurality of conductive interconnects 54 are also formed using conventional photolithographic patterning and etching techniques. The plurality of conductor interconnects 54 may be formed using doped silicon dioxide, metals, metal salicides or the like.

In FIG. 12, an optional etch stop layer 56 is then formed overlying first dielectric layer 52 and overlying the plurality of conductive interconnects 54. The optional etch stop layer 56 is formed using conventional plasma or low pressure chemical vapor deposition techniques and may be silicon dioxide, silicon nitride, silicon oxynitride, or aluminum nitride. Silicon dioxide is preferred for layer 56 and layer 56 may be etched to form sidewall spacers in FIG. 12. The layer 56 is also used to compensate for contact misalignment to the regions 54. If the air regions 60 of FIG. 13 are exposed to contact openings as illustrated in FIG. 14 and a highly conformal metallic depositions process is used, the electrical short circuiting may result. To avoid this electrical short circuit problem, the spacers or layer 56 provides the additional benefit of compensating for photolithographic contact alignment so that the air gaps are either not exposed or not substantially exposed resulting is metal deposition problems.

In FIG. 13, a second dielectric layer 58 having a low dielectric constant is formed overlying etch stop layer 56 to form air gaps 60 between portions of etch stop layer 56 and second dielectric layer 58. More specifically, as shown in FIG. 13, air gap 60 are formed between conductive interconnects 54 that are closely spaced to one another where "closely-spaced" is a function of the stiffness of the polymer backbone of the spin on resin used for layer 58. In addition, air gap 60 may also be formed along the sidewalls of a given conductive interconnect 54, as also illustrates in FIG. 12, thereby forming air spacers. In one embodiment, dielectric 58 is PPQ having a dielectric constant of less than or equal to 3.5. After layer 58 is spun on to etch stop layer 56, dielectric layer 58 is annealed at a temperature ranging from 100-250°C for approximately 30 minutes. Alternatively, dielectric layer 58 may be a pre-imidized polyimide having a dielectric constant less than or equal to 3.0. Thermal ramp processing or sub-atmospheric deposition may be used to avoid or at least reduce any blistering of the air gaps 60 of FIG. 13.

In FIG. 14, a third dielectric layer 62 is then formed overlying second dielectric layer 58. Dielectric layer 62 may be formed using conventional plasma or low pres-

removing a top portion of the dielectric layer (FIG. 6) to expose a top surface of at least one of the first conductive region or the second conductive region wherein the first portion of the dielectric layer remains within the gap.

2. The method of claim 1 wherein the step of forming a dielectric layer comprises:

forming a dielectric layer from a material selected from a group consisting of: HSQ, BCB, polyimide, and PAE.

3. The method of claim 1 wherein the step of forming a dielectric layer comprises:

forming the dielectric layer having a dielectric constant e wherein $e \leq 2.7$.

4. The method of claim 1 wherein the step of forming a first conductive region and a second conductive region comprises:

forming the first conductive region having a low conductive contact portion and an upper conductive interconnect portion to form an in-laid metal structure.

5. The method of claim 1 further characterised by:

removing a sacrificial dielectric layer located in the gap before formation of the dielectric layer having a dielectric constant e within the gap.

6. A method (FIGs. 7-10) for forming a semiconductor device, the method characterised in that the steps of:

forming a first dielectric layer (34);
forming contact openings (38) in first dielectric layer;
forming a second dielectric layer (40) overlying the first dielectric layer wherein the second dielectric layer bridges the contact openings to form contact air gaps (38);
forming openings through the second dielectric layer (40) to expose the contact air gaps and form interconnect trenches (41); and
forming conductive material (48 or 49) within the contact air gaps (38) and the interconnect trenches (41) to form a conductive interconnect wherein conductive material in the interconnect trenches are separated by the second dielectric layer (40).

7. The method of claim 6 wherein the step of forming the second dielectric layer comprises:

forming the second dielectric layer as a low dielectric constant material having a dielectric constant e wherein $e \leq 2.7$.

8. The method of claim 7 wherein the step of forming the second dielectric layer comprises:

forming the second dielectric layer as a spin-on polyimide.

9. An method (FIGs. 11-15) for forming a semiconductor device, the method characterised in that the steps of:

forming a plurality of separated conductive members (54) wherein adjacent separated conductive members in the plurality of separated conductive members are separated by gaps (60); and
forming a first dielectric layer (58), via a spin-on process, overlying the plurality of separated conductive members whereby at least one of the gaps is bridged by the first dielectric layer to form at least one air region (60), wherein the at least one air region has a dielectric constant less than 2.0 and improves isolation between at least two separated conductive members in the plurality of separated conductive members.

10. A method (FIG. 16) for forming an integrated circuit structure characterised in that the steps of:

providing a semiconductor substrate;
forming a first dielectric layer (62) overlying the semiconductor substrate;
forming a plurality of conductive members (64) overlying the first dielectric layer(62), wherein the plurality of conductive members are separated by a first distance X;
depositing a nonconformal dielectric layer (66) overlying the plurality of conductive member, wherein the nonconformal dielectric layer is deposited using plasma enhanced chemical vapor deposition and forms a sealed void region between at least two of the conductive members in the plurality of conductive members, the sealed void region spanning at least 50 percent of the first distance X; and
forming a second dielectric layer (70), the second dielectric layer overlying the sealed void region and the first dielectric layer.

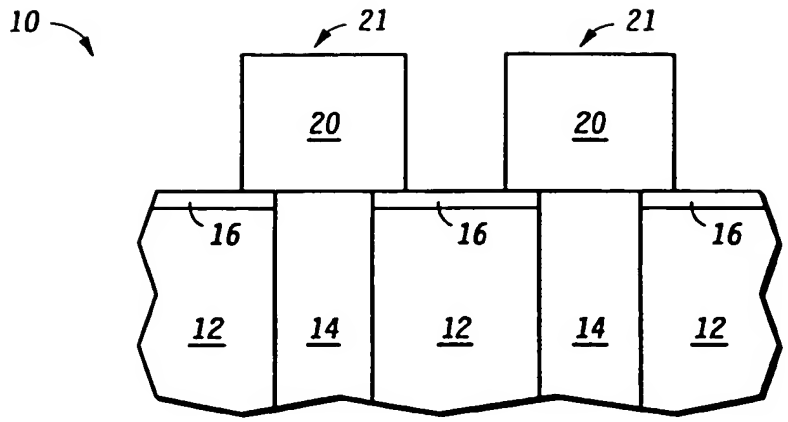

FIG.4

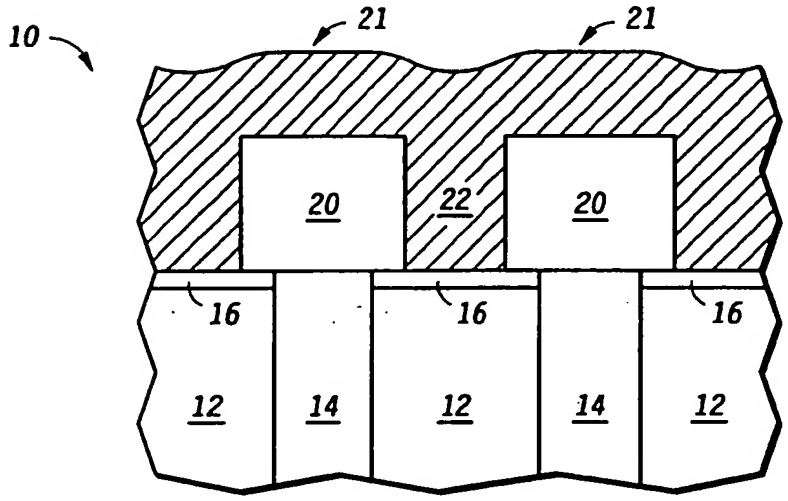

FIG.5

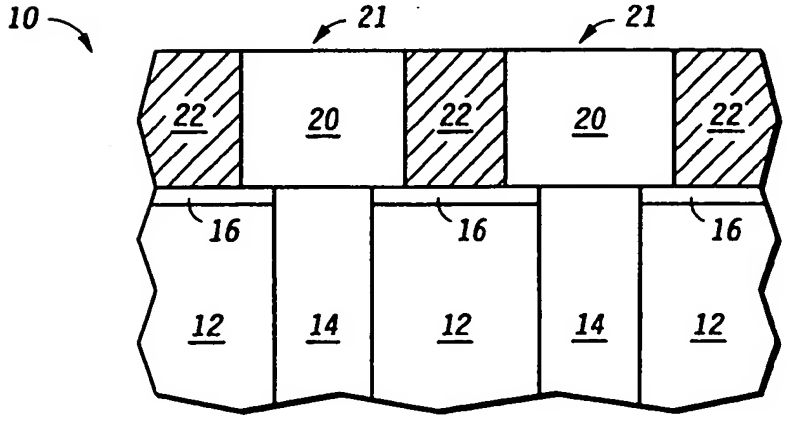

FIG.6

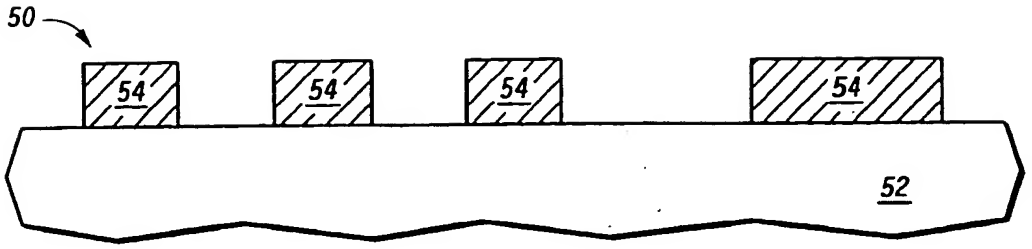

FIG.11

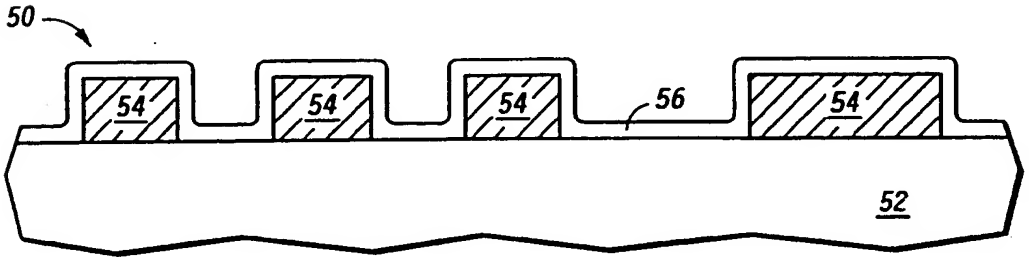

FIG.12

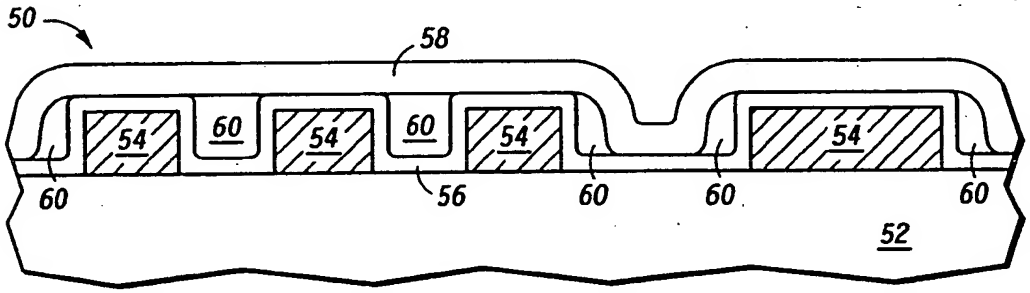

FIG.13

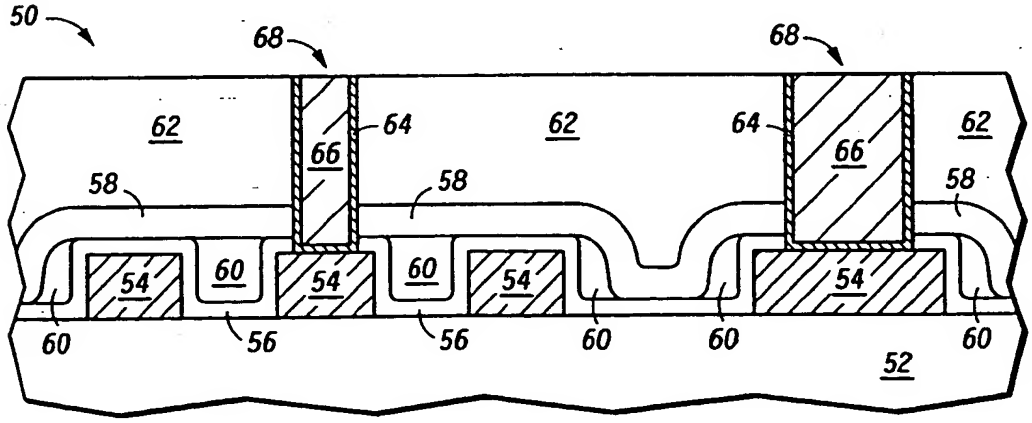

FIG.14

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(11) EP 0 834 916 A3

(12) **EUROPEAN PATENT APPLICATION**

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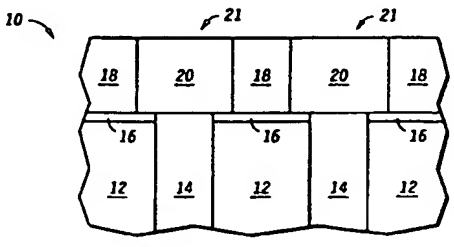

FIG.3

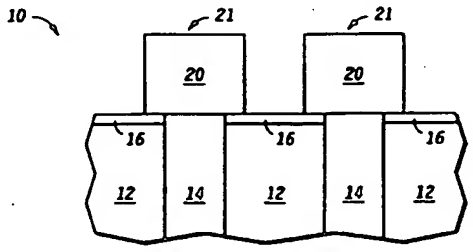

FIG.4

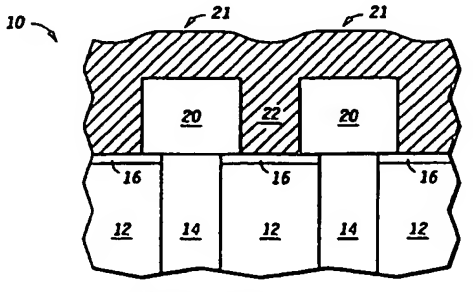

FIG.5

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EUROPEAN SEARCH REPORT

Application Number
EP 97 11 6851

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	WO 96 19830 A (ADVANCED MICRO DEVICES INC) 27 June 1996 * page 1, line 14 - line 26 * * page 2, line 11 - line 31 * * page 3, line 24 - page 5, line 19; figures 1-6 *	1-5	H01L21/768 H01L23/522 H01L23/532
X	US 5 510 293 A (NUMATA KEN) 23 April 1996 * column 1, line 21 - line 53 * * column 1, line 62 - line 67 * * column 2, line 3 - line 6 * * column 5, line 11 - line 55; figures 3A,3B,4A-4C * * column 5, line 66 - column 6, line 16; figures 6A-6D * * column 6, line 26 - line 37 *	1-3	
X	EP 0 701 277 A (TEXAS INSTRUMENTS INC) 13 March 1996 * column 2, line 42 - column 3, line 11 * * page 4, line 41 - page 5, line 8; figure 2 * * page 5, line 12 - line 27; figure 4 * * page 5, line 33 - line 41; figures 7,8 * * page 5, line 46 - line 56 *	1-3	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A		5	
X	EP 0 684 642 A (TEXAS INSTRUMENTS INC) 29 November 1995 * page 2, line 3 - line 22 * * page 2, line 55 - page 3, line 2 * * page 3, line 23 - line 25 * * page 6, line 32 - column 41, line 6A-6C * * page 8 *	1,3	
A		4	

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~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
BERLIN	5 May 1998	Klopfenstein, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

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EUROPEAN SEARCH REPORT

Application Number
EP 97 11 6851

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	WO 87 04858 A (PLESSEY OVERSEAS) * page 2, line 12 - page 3, line 14 * * page 4, line 22 - page 6, line 2; figures 1-4 * ---	6-8	
A	US 5 407 860 A (STOLTZ RICHARD A ET AL) 18 April 1995 * column 1, line 66 - column 2, line 28 * * column 2, line 65 - column 3, line 39; figures 1-6 * ---	6-8	
A	MINAMIHABA G ET AL: "DOUBLE-LEVEL CU INLAID INTERCONNECTS WITH SIMULTANEOUSLY FILLED VIA-PLUGS" INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS, 21 August 1995, pages 97-99, XP000544574 * page 97, paragraph 2 - page 98, paragraph 4; figures 2,3 * -----	6	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
BERLIN	5 May 1998	Klopfenstein, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 97 11 6851

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-5

A method for isolating a first and a second laterally separated conductive regions, by filling a gap between said two regions with a dielectric layer having a dielectric constant e lower than 3.5 (Figs.1-6).

2. Claims: 6-8

A method for forming isolated separated conductive interconnects by etching interconnection trenches in portions of a second dielectric layer, said trenches also exposing air gaps formed in a previous step of patterning an underlying first dielectric layer and filling these trenches and air gaps by conductive material (Figs.7-10)

3. Claim : 9

A method for isolating adjacent separated conductive members by forming, via a spin-on process, a dielectric layer overlying the separated conductive members, without filling the space separating said members, thus bridging said space to form an air gap (Figs.11-15)

4. Claim : 10

A method for isolating adjacent separated conductive members by forming, via a PECVD process, a non-conformal dielectric layer overlying the separated conductive members, thus forming a sealed void between at least two of the conductive members, the sealed void spanning at least 50% of the distance between the two conductive members (Fig.16).

DOCKET NO: 2dP-INFN 10176
SERIAL NO: _____
APPLICANT: Gabriele Biase et al.

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